DCG MEMO # 403

TO: Distribution
FROM: R.A. D'Angelo
DATE: January 3, 1972
SUBJECT: Simulator Error

It has been discovered that the Simulator, since the changeover from the Honeywell 1800, has not correctly set up its internal overflow check routines when executing a CCS Q instruction in the case that Q contains overflow. The overflow bit is placed in the A register. The CCS instruction itself is executed correctly, but the simulator doesn't turn on its overflow check switch and thus the fact that A contains overflow is ignored by the simulator. This condition continues until an instruction that could possibly cause overflow is executed; i.e., an add, whereupon the simulator checks for overflow, finds it, and continues checking until the overflow disappears. Apparently the only error that can result from this is in the decision whether or not to skip an instruction after a TS instruction. If the simulator is still not checking for overflow, the instruction after the TS will be executed which is an error condition.

To summarize, the conditions required to cause an error in the simulator are:

Q contains overflow
a CCS on a Q is done
no arithmatic or XCH instructions are done
a TS is done

The simulator had the error fixed at 11:32 a.m. on 1/3/72.